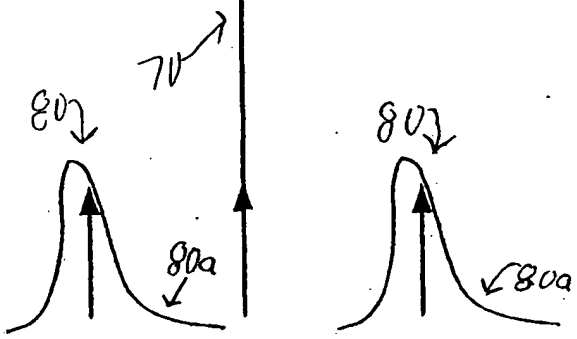
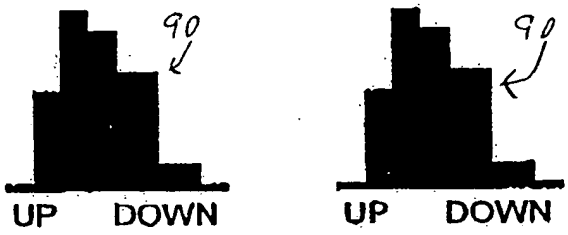
Eye diagram
FIG. 1A



Jitter histogram &
Sampling clocks
FIG. 1B

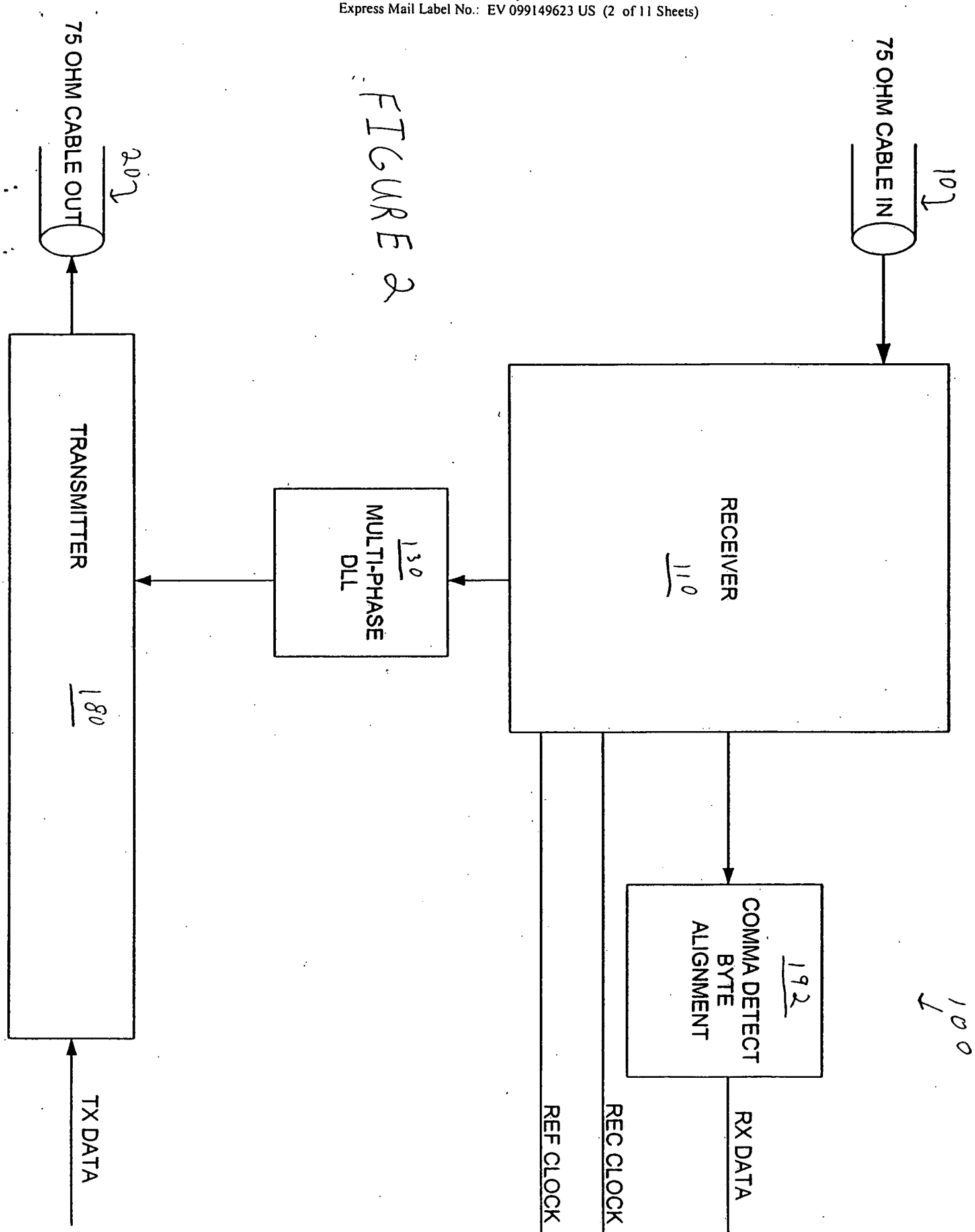


# of UP pulses &
# of DOWN pulses
FIG. 1C

"PRIOR ART"

BEST AVAILABLE COPY

FIGURE 2


75 OHM CABLE IN
101
75 OHM CABLE OUT
202
RECEIVER
110
TRANSMITTER
180
130
MULTI-PHASE
DLL
192
COMMA DETECT
BYTE
ALIGNMENT
100
REF CLOCK
REC CLOCK
RX DATA
TX DATA

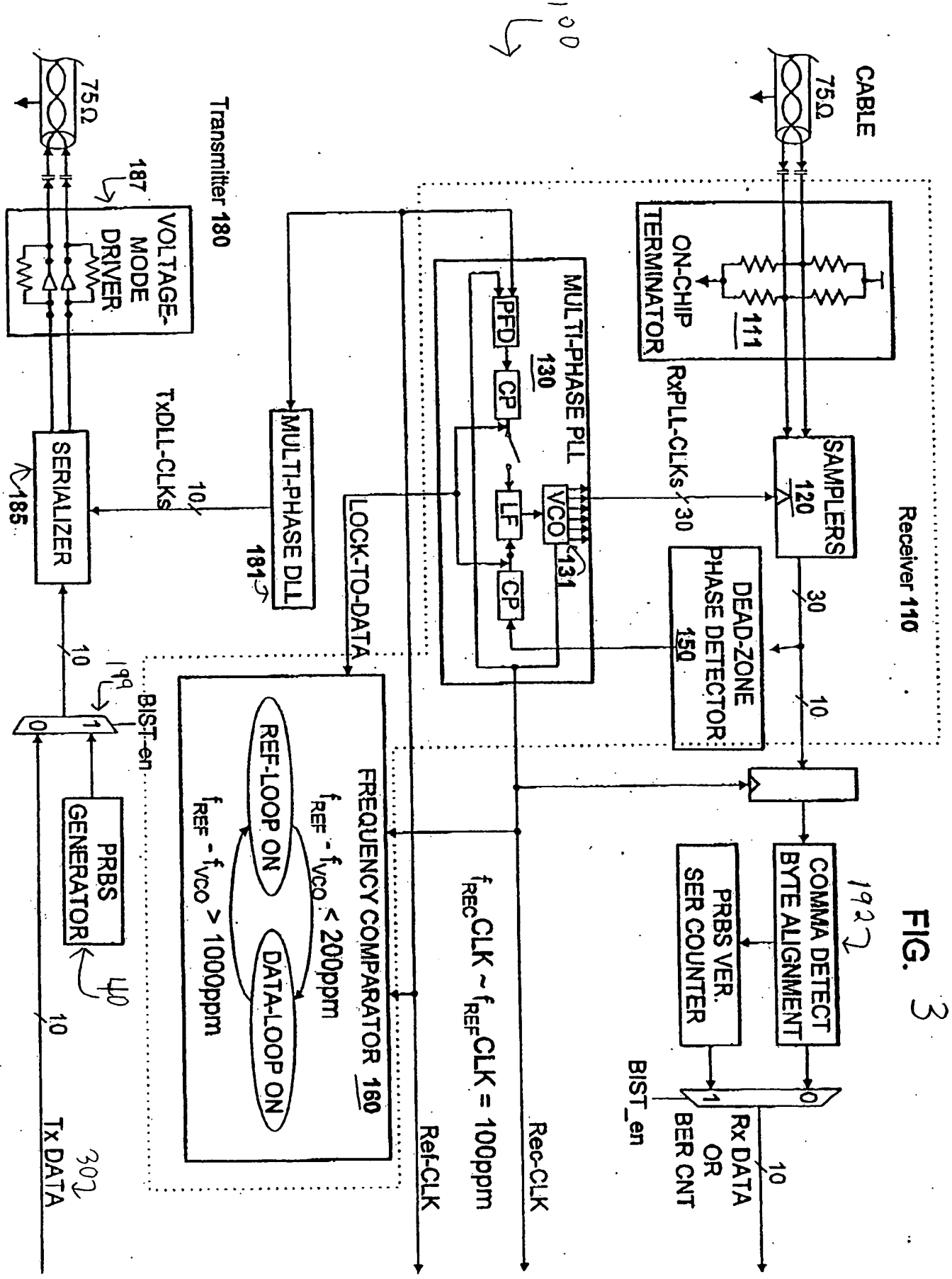

100
CABLE
75Ω
Receiver 110
ON-CHIP TERMINATOR
111
SAMPLERS
120
RxPLL-CLKs
30
MULTI-PHASE PLL
130
PFD
CP
LF
VCO
131
CP
DEAD-ZONE PHASE DETECTOR
150
LOCK-TO-DATA
MULTI-PHASE DLL
181
TxDLL-CLKs
10
SERIALIZER
185
Transmitter 180
VOLTAGE-MODE DRIVER
187
75Ω
FREQUENCY COMPARATOR 160
REF-LOOP ON
DATA-LOOP ON
$f_{REF} - f_{VCO} < 200ppm$
$f_{REF} - f_{VCO} > 1000ppm$
$f_{REC}CLK \sim f_{REF}CLK = 100ppm$
Rec-CLK
Ref-CLK
BIST_en
199
PRBS GENERATOR
40
Tx DATA
302
COMMA DETECT BYTE ALIGNMENT
PRBS VER. SER COUNTER
192
Rx DATA OR BER CNT

FIG. 3

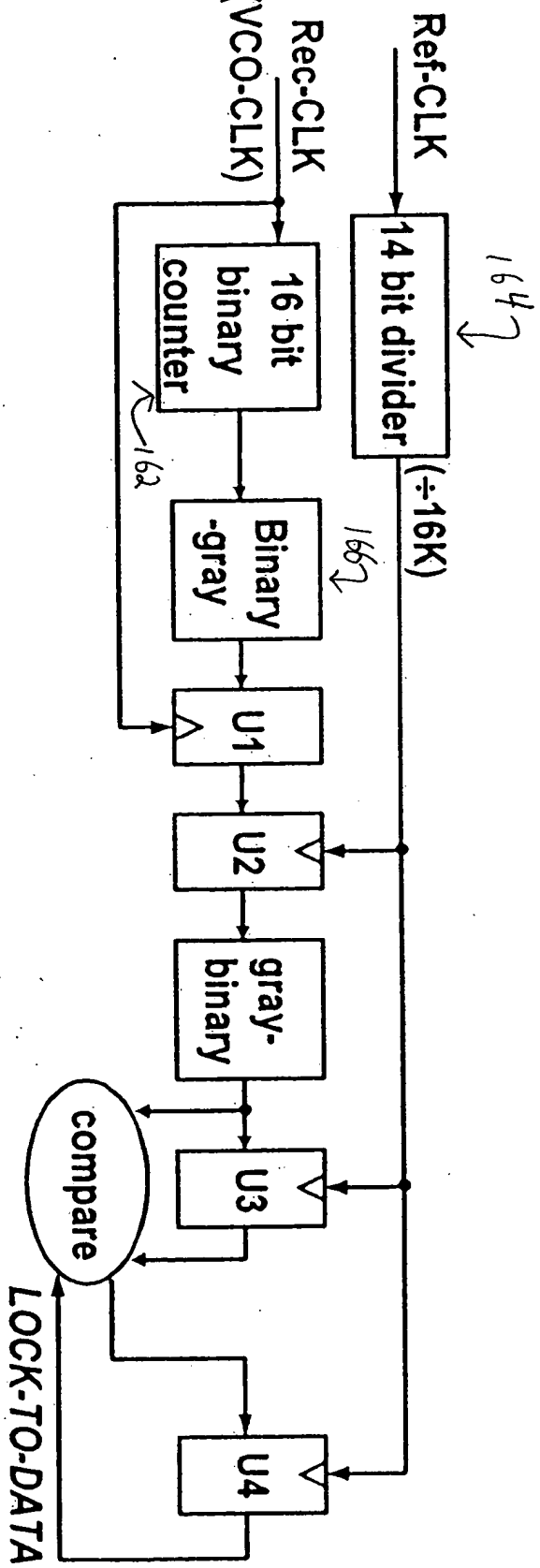
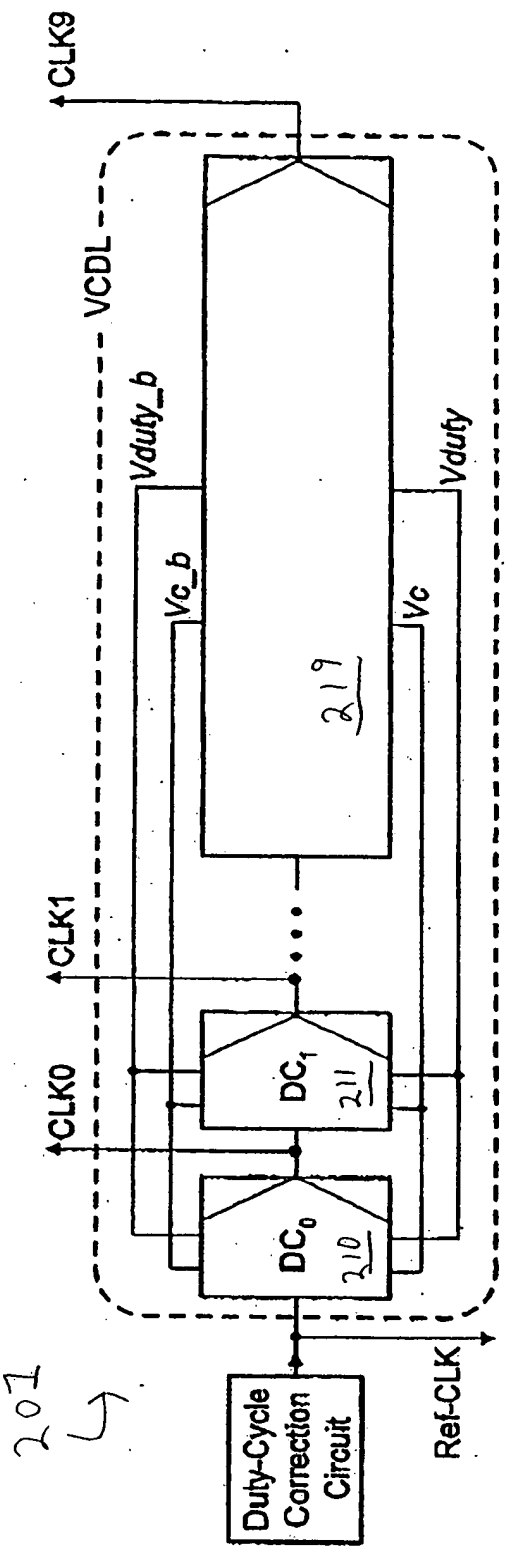

Ref-CLK
Rec-CLK
(VCO-CLK)
14 bit divider
(÷16K)
16 bit binary counter
Binary -gray
U1
U2
gray-binary
compare
U3
U4
LOCK-TO-DATA
160
162
164
166

FIGURE 4

FIG. 5A


CLK9
VCDL
Vduty_b
Vc_b
Vc
Vduty
219
CLK1
CLK0
DC1
211
DC0
210
201
Duty-Cycle Correction Circuit
Ref-CLK

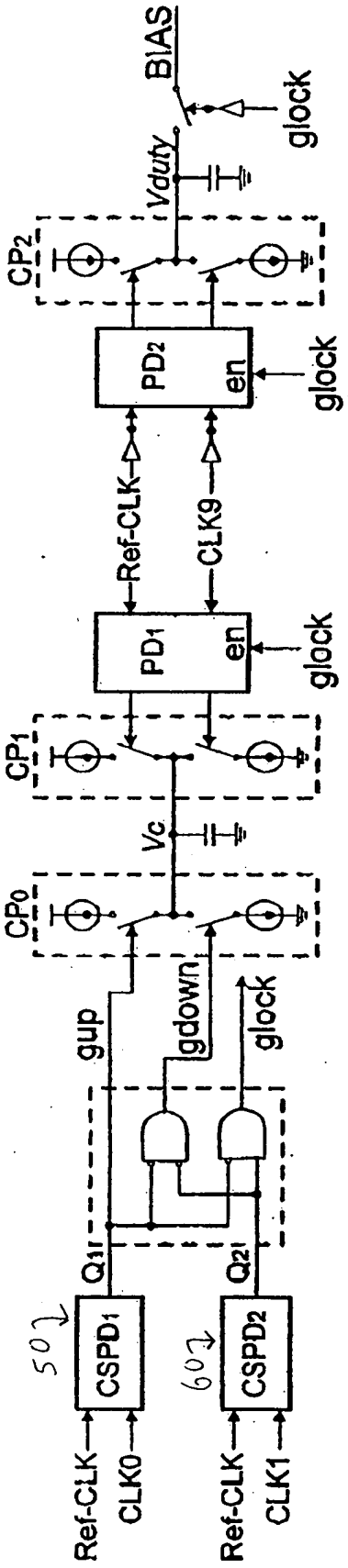
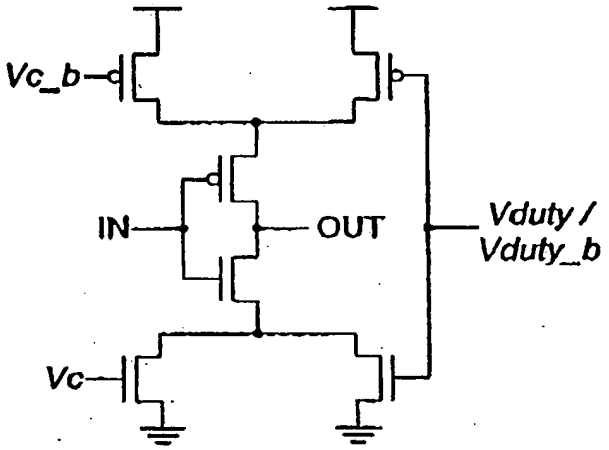

BIAS
glock
Vduty
CP2
PD2
en
glock
Ref-CLK
CLK9
PD1
en
glock
CP1
Vc
CP0
gup
gdown
glock
Q1
Q2
501
CSPD1
601
CSPD2
Ref-CLK
CLK0
Ref-CLK
CLK1

FIG. 5B



210

FIG. 5C

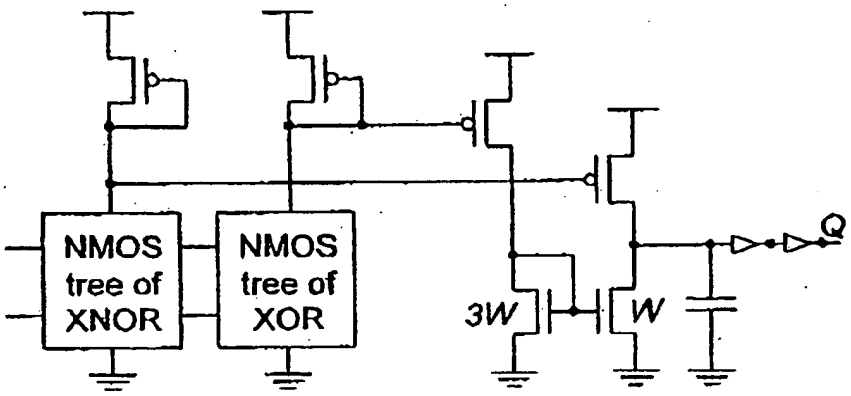


FIG. 5D

50

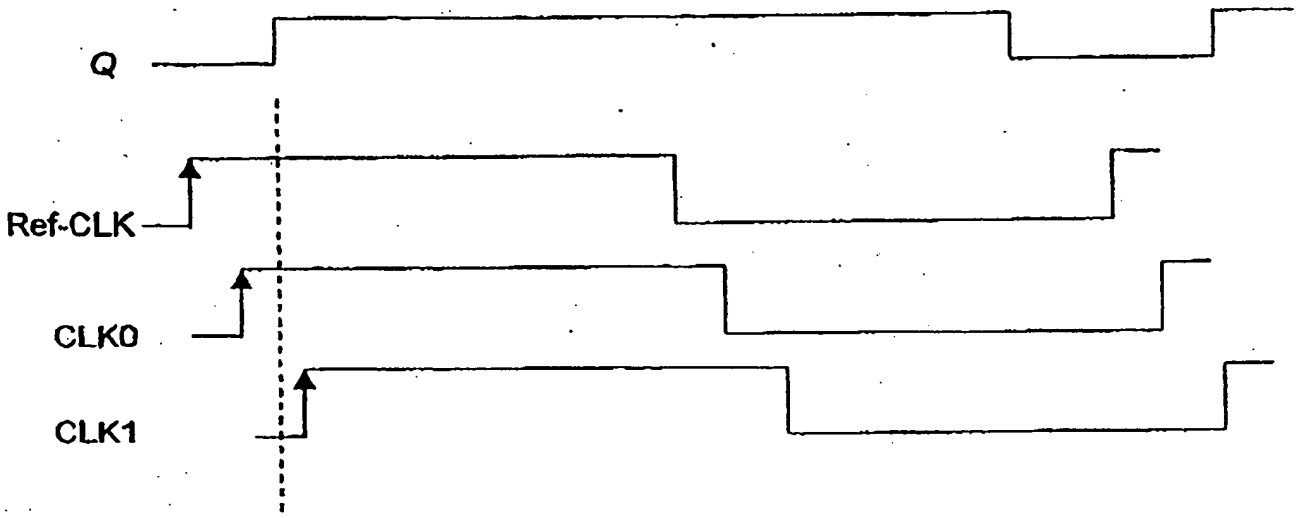
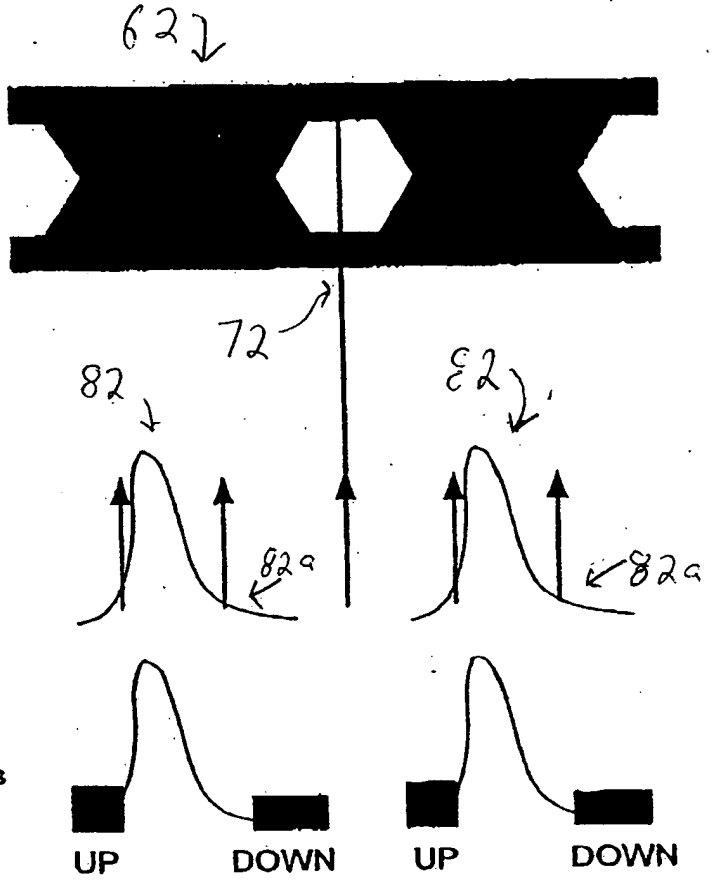


FIG. 5E

Eye diagram
FIG. 6A

Jitter histogram &
Sampling clocks
FIG. 6B

# of UP pulses &
# of DOWN pulses
FIG. 6C



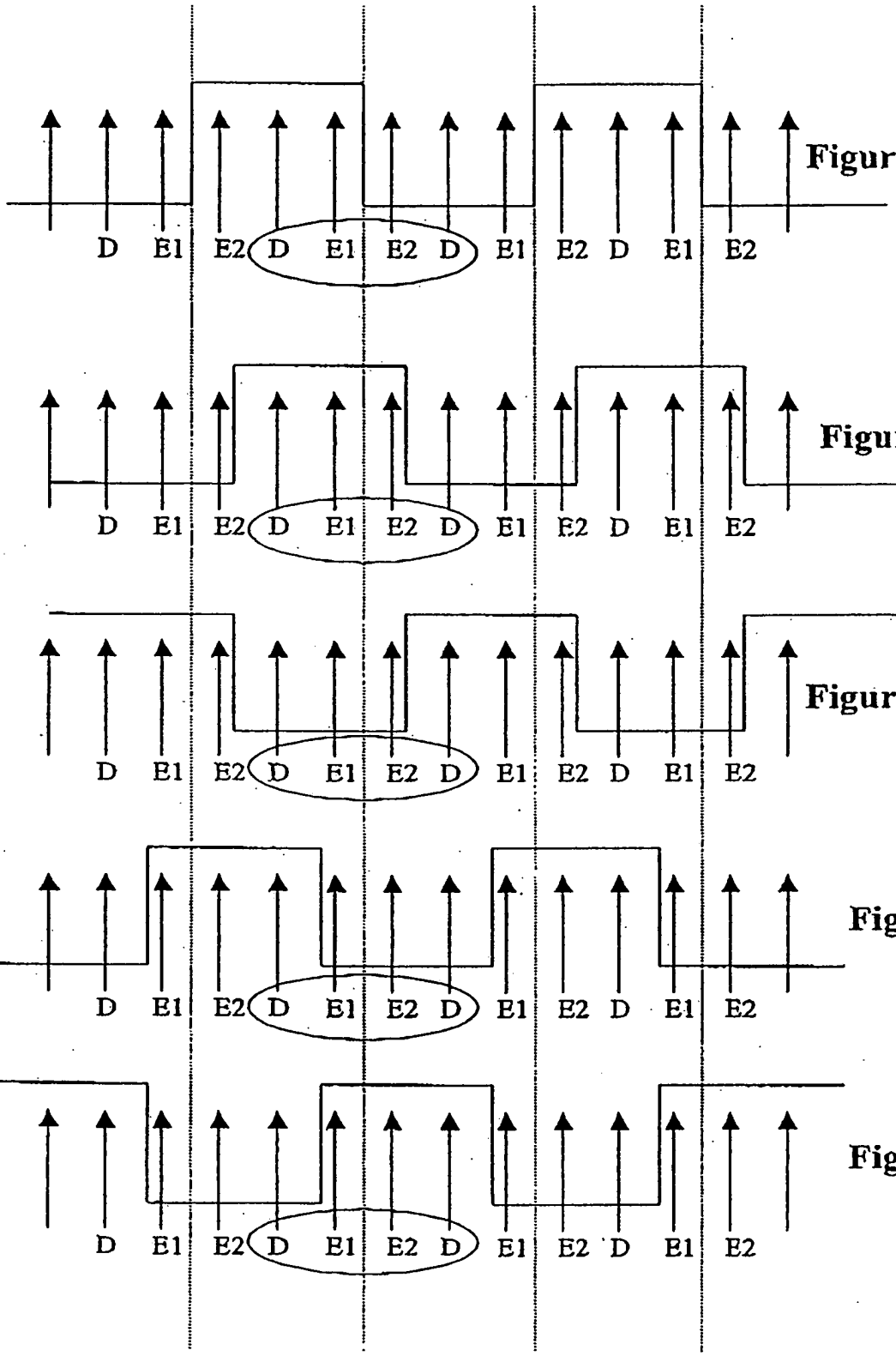


Figure 7A

Figure 7B

Figure 7C

Figure 7D

Figure 7E

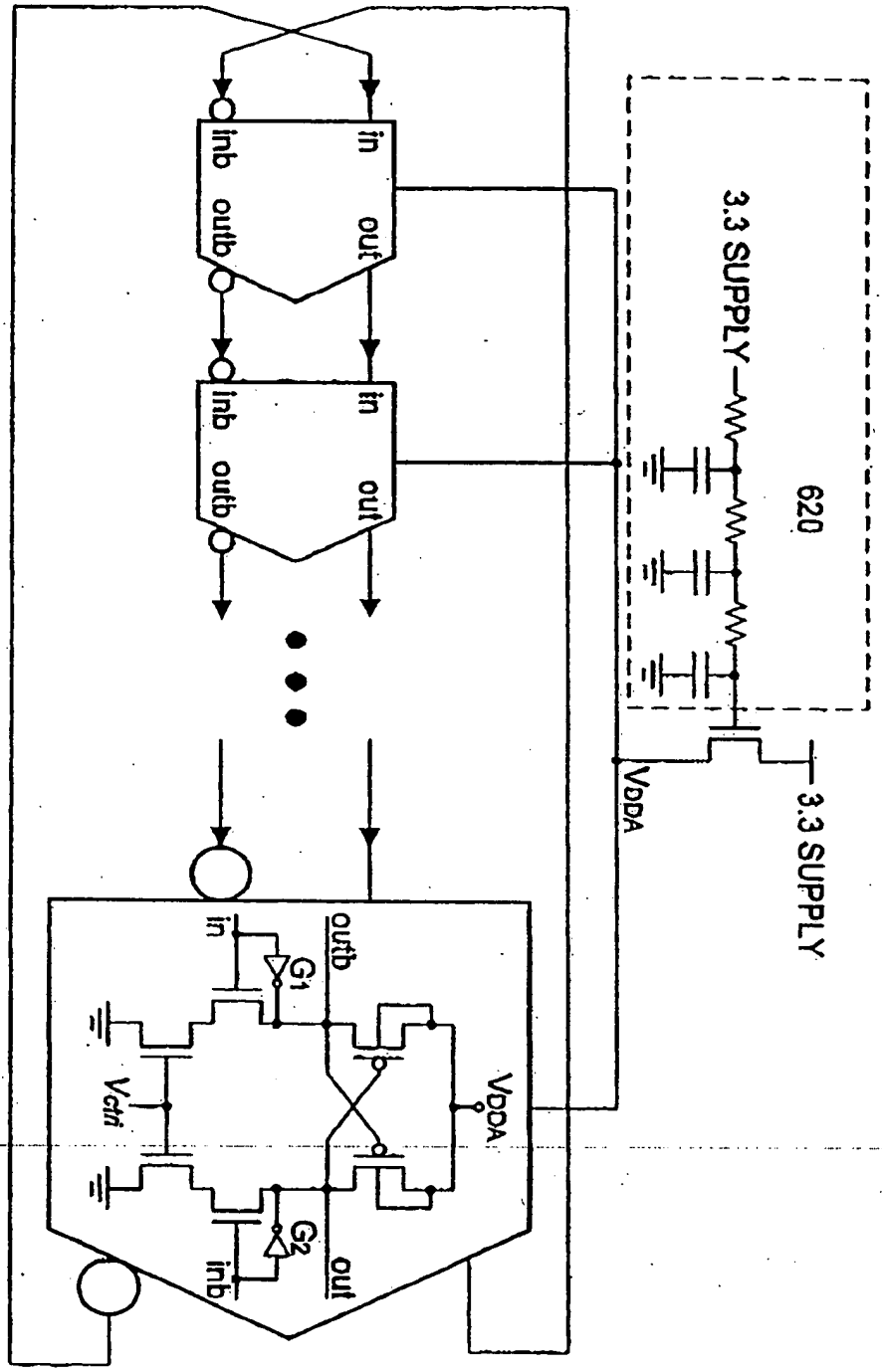

inb
outb
in
out
3.3 SUPPLY
620
VDDA
3.3 SUPPLY
in
outb
G1
Vctrl
VDDA
G2
inb
out

FIG. 8